insulator, wherein a barrier energy between the amorphous silicon carbide (a-SiC) gate insulator

and the floating gate electrode is less than 3.3 eV;

    reading the data stored on the floating gate electrode by placing a read voltage on the

control line and detecting the current in the floating gate transistor at the data line; and

    erasing the floating gate transistor by applying an erase voltage to the floating gate

transistor.

60.   (New) The method of claim 59, further comprising refreshing the charge placed on the

floating gate electrode.

61.   (New) The method of claim 60 wherein refreshing the charge placed on the floating gate

electrode further comprises refreshing the charge at regular time intervals.

62.   (New) The method of claim 59 wherein erasing comprises erasing the floating gate

transistor by applying an erase voltage to the floating gate transistor which is less than 12 Volts.

63.   (New) The method of claim 59 wherein storing data further comprises storing data on the

floating gate electrode in the floating gate transistor by providing a control voltage on the control

line and a write voltage on the data line such that charge is carried from a channel between a

source region and a drain region in a silicon substrate to the floating gate electrode through the

amorphous silicon carbide (a-SiC) gate insulator.

REMARKS

    In response to the Office Action mailed July 9, 1999, the applicant requests

reconsideration of the above-identified application in view of the following remarks. Claims 19-

21, 28-38, and 43-50 are pending in the application. Claims 28-38, 48, and 50 are allowed.

Claims 19-21, 43-47, and 49 are rejected. Claims 43, 44, 47, and 48 will be amended, and new

claims 51-63 will be added upon entry of the present amendment. Claim 48 was allowed and the

amendment to claim 48 was not made in response to a rejection but rather to reflect antecedent

basis in claim 47.

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